Amendments to the Specification

Please amend the following portions of the specification as shown below:

After paragraph [0011] of the specification as filed, please add the following paragraphs:

"FIG. 3 illustrates a block diagram of an exemplary digital signal processor according to embodiments of the present invention.

FIG 4 illustrates a block diagram of an exemplary reset synchronization system according to embodiments of the present invention.

FIG 5 shows a block diagram of a I/O multiplexer system according to embodiments of the present invention.

FIG. 6 illustrates a block diagram of an exemplary adaptable strapping system according to an embodiment of the present invention.

FIG. 7 illustrates a block diagram of an exemplary multi-channel audio interconnect system.

FIG. 8 illustrates a block diagram of an exemplary FM demodulation system.

FIG. 9 illustrates a block diagram of an exemplary a video data stream front end processor.

FIG. 10 illustrates a block diagram of an exemplary packet substitution module.

FIG. 11 illustrates a block diagram of an exemplary media processing system.

FIG. 12 illustrates a block diagram of an exemplary video system having an artificial time stamp module.

FIG. 13 illustrates a block diagram of an exemplary RAM implementation of a color lookup table and gamma correction function.

FIG. 14 illustrates a block diagram of an exemplary 2D adaptive comb filter.

FIG. 15 illustrates a block diagram of an exemplary timing generator.

FIG. 16 illustrates a block diagram of an exemplary system for detecting and decoding teletext message sequences.

FIG. 17 illustrates a block diagram of an exemplary copy-protection filter.

FIG. 18 illustrates a block diagram of an exemplary signal mode detection system.

Please amend paragraph [0023]:

"In an embodiment, IF demodulator 202 can optionally include a FM demodulation system for approximating y(n)=1/(x(n)), where x(n)=I2(n)+Q2(n). An exemplary FM demodulation system 800 is illustrated in FIG. 8. FM demodulator 800 can include a filter 806 (e.g., a Hilbert Filter) that generates a quadrature-phase signal Q(n) 804 from I(n) 810. The signals I(n) 810 and Q(n) 804 are input into an FM demodulation system 802, which produces FM(n) output signal 812. . . . . A secondary audio program (SAP) signal received must be processed . . . ."

Please amend paragraph [0028]:

"~~The~~ An exemplary video data stream front end processor system 900 as illustrated in FIG. 9 includes synchronizers 910A-910E, parsers 920A-920E, demultiplexers 930A and 930B, and an input buffer 940. . . . The video data stream

front end processor is further taught in co-pending application, U.S. Patent Application No. 10/640,682 ~~10/640,684~~, filed Aug. 14, 2003, which is herein incorporated by reference in its entirety."

Please amend paragraph [0031]:

". . . ~~The~~ An exemplary packet substitution module system 1000 as illustrated in FIG. 10 includes a set of packet buffers 1010A - 1010D that buffer packets to be substituted into the data stream. The packet substitution module system 1000 also includes a multiplexer 1030 that obtains packets from the set of packet buffers 1010A-1010D and substitutes packets into the data stream. The operation of the multiplexer 1020 is controlled by a packet substitution controller 1030. A direct memory access engine provides packets for insertion to the packet buffers based on a link list buffer control that is coupled the direct memory access engine. . . . ."

Please amend paragraph [0034]:

". . . . ~~The~~ An exemplary media processing system 1100 as illustrated in FIG. 11 includes a processor 1102, a set of timestamp insertion modules 1104A - 1104N coupled to the processor 1102. The number of timestamp insertion modules 1104 would be equal to the number of program channels being processed. Each timestamp insertion module 1104 would include a local program reference clock, a synchronizer that synchronized the local program reference clock to a clock of a device transmitting the program being processed, a local program timestamp generator, and an input buffer 1108 may be coupled to the timestamp insertion modules. . . ."

Please amend paragraph [0038]:

"~~The~~ An exemplary 2D adaptive comb filter 1400 as illustrated in FIG. 14 includes a band limiting filter 1402, a decision stage 1404, a blending stage 1406, and a processor 1410. . . . . "

Please amend paragraph [0039]:

"An artificial time stamp module generates timestamps that are inserted into the DV25 or DV50 information, thereby facilitating decoding by an MPEG signal processor. An exemplary artificial time stamp module including system time clock 1212 and time control device 1210 is illustrated in FIG. 12 illustrating a video system 1200. A data transport device 1208 controls the transmission of data within system 1200. A time control device 1210 can be used to generate and associate time stamp information with the data. A system time clock 1212 can be used in one embodiment in conjunction with the time control device to generate time stamp information. A storage device 1214 is used to store the pseudo MPEG information and other data received by data transport device 1208. A decoder 1216 is used to decode the pseudo MPEG information. A controller 1218 can be used to control one or more components of system 1200. Output device 1244 outputs the decoded pseudo MPEG information based on the artificial time stamp information. An artificial time stamp module is further taught . . . ."

Please amend paragraph [0040]:

" . . . ~~The~~ An exemplary teletext decoder system 1600 as illustrated in FIG. 16 includes a correlator 1630, a sine wave generator 1640, ~~two~~ a first time window generator[[s]] 1610 and a second time window generator 1620, a phase detector 1650, a framing code search engine 1660, and a match filter 1670. . . ."

Please amend paragraph [0042]:

" . . . ~~The~~ An exemplary combined color look-up and gamma correction system includes an input matrix configured to receive first and second type pixel data. Memory is coupled to the input matrix and configured to associate one of the first and second type pixel data with the stored CLUT parameters and associate the other of the first and second type pixel data with the stored gamma correction parameters. For example, an exemplary RAM memory system 1300 is illustrated in FIG. 13. System 1300 is configured to perform both CLUT and gamma correction functions, in accordance with the present invention. System 1300 includes an input matrix 1301, a memory section 1302, and an output matrix 1303 configured to receive the input pixel words 1390, 1391, 1393, and 1394. The memory section 1302 includes RAMs 1304, 1305, 1306 and 1308. The RAMs 1305, 1306, and 1308 are respectively connected to input multiplexing devices 1310, 1312 and 1314. When configured for the gamma correction mode, individual color components 1380, 1382 and 1384 are provided as inputs to respective multiplexing devices 1310, 1312, and 1314 and along data lines 1348 as inputs to respective multiplexing devices 1326, 1328, and 1330. Four data paths 1322 are coupled to multiplexing device 1324. An output of the multiplexing device 1324 is provided to a multiplexing device 1340.

Multiplexing device 1342 receives one input from the multiplexing device 1340 and other inputs from the multiplexing devices 1326, 1328 and 1330, to provide an output 1344. "

Please amend paragraph [0046]:

" . . . ~~The~~ An exemplary timing generator 1500 as illustrated in FIG. 15 includes a set of microsequencers 1505A-1505G, a programmable combinational logic (PCL) module 1510, shared memory, an arbiter 1530 for sharing of memory by the microsequencers 1505, stacks 1540 containing registers for microsequencer 1505 control, and a control interface. . . . ."

Please amend paragraph [0047]:

" . . . The MPAA HDTV copy protection filter system provides an efficient system to reduce the resolution of a digital video signal to comply with the MPAA copy protection standards by integrating copy protection filters with elements of video encoder 218. An exemplary MPAA HDTV filter system is illustrated in FIG. 17. FIG. 17 shows a block diagram of an exemplary system 1700 included in, for example, a set-top box or a TV-on-a-chip system. System 1700 includes a compositor 1702 and a video encoder ("VEC") 1704. Compositor 1702 accepts an input video signal 1706 and an input graphics signal 1708. Compositor outputs composite video signal 1710. VEC 1704 includes a sync timing circuit 1712, a bandpass filter 1714, and a digital-to-analog converter ("DAC") 1716, along a first data path 1718. In one embodiment, VEC 1704 also includes a digital visual interface ("DVI") transmitter

1720 on a second data path 1722. A copy-protection filter 1750 may be inserted into one or more of the video signal data paths 1706, 1710, 1718, and 1722 (shown in 1710 only. In an embodiment, the copy-protection filter is a low-pass horizontal filter. . . ."

Please amend paragraph [0051]:

" . . . ~~The~~ An exemplary signal mode detection system 1800 as illustrated in FIG. 18 ~~can~~ includes a first bandpass filter 1802, a first envelope tracker 1804 coupled to the first bandpass filter 1802, a second bandpass filter 1806, a second envelope tracker 1808 coupled to the second bandpass filter 1806, and a decision circuit 1810 coupled to both the first and second envelope trackers 1804 and 1808. . . ."

Please amend paragraph [0053]:

"In an embodiment, audio decoder 220 can optionally include a digital signal processor (DSP) decoder 300, such as one illustrated in FIG. 3, having an execution unit 302, a memory 306, an address generator 308 and an instruction set that can be used to decode input signals. . . ."

Please amend paragraph [0062]:

". . . . ~~The~~ An exemplary reset synchronization system 400 as illustrated in FIG. 4 showing a reset generator 404 and a circuit 418. A local clock A 412 drives circuit 418 and clock B 406 drives reset generator 404. A reset synchronizer

including synchronizing circuitry 402 receives a reset signal 408 and local clock A 412. The synchronizing circuitry 402 outputs a synchronized reset signal 422 that is used to reset circuit 418 or portions thereof. Thus, a reset synchronization system includes a local clock terminal 420, a reset terminal 424, a synchronized reset output terminal 422, and synchronizing circuitry 402 coupled between the clock terminal 420, the reset terminal 424, and the synchronized reset output terminal 422. . . . "

Please amend paragraph [0064]:

"~~The~~ An exemplary I/O multiplexing system 500 as illustrated in FIG. 5 includes an input/output device including a bi-directional pad, function blocks 502A and 502B coupled to the I/O device and an I/O multiplexing module 506 that controls transmission of the signals between the function blocks 502A and 502B and the I/O device using a controller. The I/O multiplexing module 506 can include a data I/O multiplexer and an enable I/O multiplexer coupled to the controller."

Please amend paragraph [0067]:

". . . An exemplary ~~The~~ adaptable strapping system 600 as illustrated in FIG. 6 includes a control system 608 that controls a mode of TVOC 200, an initialization system 604 that transmits a signal to the control system 608 to initialize TVOC 200, an internal strapping system 606 that transmits a signal to the control system 608 that can be ~~sued~~ used to place TVOC 200 in a first state, and an override system 610that transmits a second signal to the control system to place TVOC 200 in a second state. . . ."

Please amend paragraph [0070]:

". . . . ~~The~~ An exemplary multi-channel audio interconnect system 700 as illustrated in FIG. 7. System 700 includes an encoder positioned within the transmitting module and configured to convert audio data requiring transmission into two-line audio information segments. As shown in FIG. 7, the system 700 includes the 3-line data bus 706 for transferring input audio information 715 between the transmitter 702 and the receiver 704. In order to accommodate this information transfer, the I2S protocol suite may be used for formatting the clock bit data transferred along the clock line 708, the word select data 710, and the serial data stream 712.

Transmitter 702 of FIG. 7 includes a standard audio encoder 713 configured for converting received data 715 into a format for transfer across the data bus 706. The receiver 704 includes a conventional audio decoder 714 configured to decode the encoded audio data received via the data path 706. The encoder 713 can be used, for example, to convert received audio PCM data into an I2S format or the popular Sony/Philips digital interface (SPDIF) format. . . . The multi-channel audio interconnect system is further taught in co-pending application, U.S. Patent Application No.: 10/646,833 ~~(Attorney Docket No. 19/646,833)~~, filed Aug. 25, 2003."